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Short communication

DSP based inverter control for alternate energy systems

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Abstract

This paper presents a DSP based algorithm to control inverters used in interfacing alternate energy systems with the electric utility. Since a constant and ripple free dc bus voltage is not ensured at the output of alternate energy sources, the main aim of the proposed algorithm is to make the output of the inverter immune to the fluctuations in the dc input voltage. In this paper a modified space vector pulse width modulation (SVPWM) technique is proposed which will maintain the quality of the ac output of the inverter, regardless of the ripple present at the inverter input. The principle is explained qualitatively and extensive experiments have been carried out to verify and validate the proposed algorithm. A 16-bit fixed-point C2000 family DSP from Texas Instruments was used as the controller to implement the proposed control algorithm.

Keywords: Alternate energy systems; Inverter; Ripple (dc-bus voltage ripple); DSP

1. Introduction

Increasing awareness of environmental factors and limited conventional energy resources has led to a profound evolution in the way we generate electric energy. Although fossil and nuclear sources will remain the most important energy provider for many more years, flexible technological solutions that involve alternative means of energy generation need to be developed urgently. The most pronouncing breakthroughs are currently taking place for technologies, using alternate energy sources such as solar energy [1,2], wind energy [3], electro-chemical energy [4], etc. Recent developments in such technologies have shown several distinct advantages over the conventional means of energy generation. In particular, alternative resources of energy assist in the reduction of the emission of greenhouse gases and add the much-needed flexibility to the energy resources by decreasing our dependence on fossil fuels. In addition, the above sources of energy are non-polluting and renewable.

Alternate energy sources like PV systems and wind systems produce low voltage dc power. A number of solar cells, which are connected in series and parallel, constitute a photovoltaic or solar array. When such solar arrays are exposed to sunlight, they produce a dc voltage. However, partial shading of PV systems, result in "unbalanced generation" condition which contributes in producing dc voltages that are not constant [1]. In the case of wind electric systems, the wind turbine drives an ac generator, which produces three phase voltages at a frequency, which is dependent on the wind speed. The variable frequency ac voltages thus generated are then converted to dc with the help of a ac to dc converter. Also, in any practical converter system it is difficult to realize a constant and ripple free dc bus for practical constraints like unbalanced input ac supply, nonlinearity and unbalances in loads, etc. [9].

Hence, a constant and ripple free dc bus voltage is not ensured at the output of alternate energy sources. Inverters (dc to ac converter) are used in converting low-voltage dc power generated from alternate energy sources into higher-voltage ac power required for residential, industrial and commercial applications [5]. However, in order to guarantee high-quality inverter output voltage, all standard inverter control schemes are based on the assumption of an ideal dc bus (ripple free). The ripple in the dc bus is undesirable, as it causes lower order harmonics to appear in the output of single phase inverters and deteriorates the output voltage quality [6]. In a three phase inverter, ripple on the dc bus causes fluctuations in the output voltage magnitude which is undesirable. A dc-link voltage, which is ripple-free to some extent, can be achieved at the expense of large dc-link filter components. But these filter components have the disadvantages of

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being bulky, unreliable and contributing to slow response and increased losses. So an alternative should be found out to make the output of the inverter immune or insensitive to the ripple present in the input.

Some attempts were made in the past to reject dc-link voltage ripple at the inverter input which require cumbersome real-time calculations that make them complicated to implement [7,8]. The ripple component of the input voltage of PWM inverters has been analyzed in [9] and it was found that the optimum reference signal with respect to the inverter input voltage ripple varies with the load power factor. But these analysis results are mostly useful in determining the specifications of the required dc filter. A cycle by cycle integral control scheme based on analog implementation is proposed in [9] for compensating non-ideal dc bus conditions. Alternatives for implementing space vector modulation with the DSP TMS320F240 is presented in [10] but none of the alternatives make the output of the inverter immune or insensitive to the ripple present in the input dc voltage.

In this paper a modified space vector pulse width modulation (SVPWM) technique is presented to compensate for the ripple present in the dc voltage obtained from alternate energy systems. The digital compensator is implemented in a digital-signal-processor (DSP) based system. Texas Instruments TMS320F243 DSP is used for the implementation. None of the earlier work has used SVPWM. Also, the technique is implemented using Texas Instruments TMS320F243 DSP which is cost effective and efficient.

2. Space vector pulse width modulation (SVPWM)

A three-phase voltage source PWM inverter system is shown in Fig. 1. For the three phase inverter, there are eight combinations (vectors) of the ON and OFF states of the inverter switches S1 through S6.

Six of these eight are non-zero base vectors (v_1 through v_6) and are shown in Fig. 2. Two other vectors not shown in the figure are v_0 and v_7, are the zero vectors corresponding to states 0 (0 0 0) and 7 (1 1 1) of the switching variables. The base vectors divide the cycle into six, 60° wide sectors. Let us assume that an arbitrary voltage V^* is to be generated by the inverter. The desired voltage V^*, located in any sector can be approximated as the linear combination of the adjacent base vectors V_x and V_y

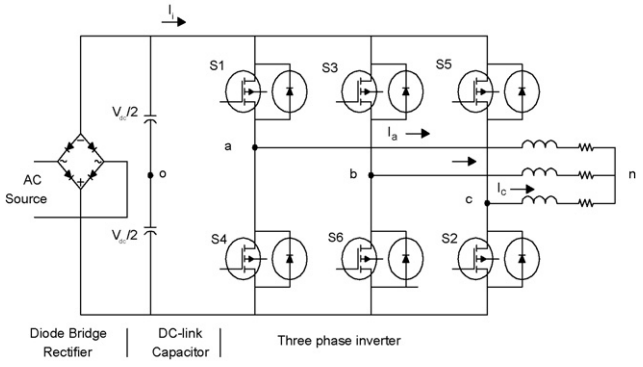


Fig. 1. A three-phase PWM inverter system.

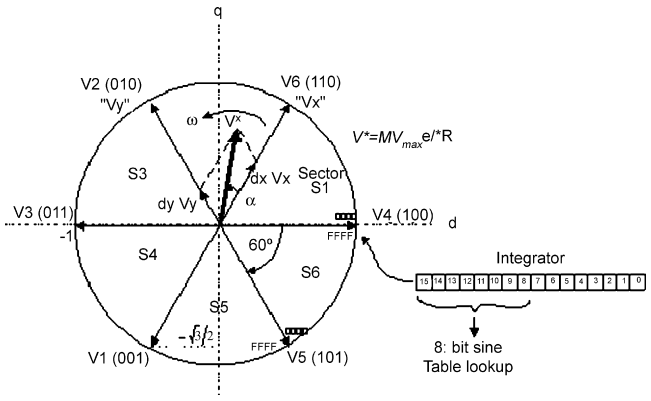


Fig. 2. Generation of reference voltage vector using base vectors.

along with one of the two zero vectors as in Eq. (1) given below:

$$V^* = d_x V_x + d_y V_y + d_z V_z \tag{1}$$

where V_z is the zero vector and d_x, d_y and d_z denote the duty ratios of states X, Y and Z within one PWM cycle. The duty ratios must add up to 100% of the PWM switching period, i.e.

$$d_x + d_y + d_z = 1 \tag{2}$$

Vector V^* in Fig. 2 can also be written as

$$V^* = MV_{\max}\, e^{j\alpha} = d_x V_x + d_y V_y + d_z V_z \tag{3}$$

where M is the modulation index and $V_{\max} = \sqrt{3}/2 V_{dc}$, is the maximum value of the desired phase voltage.

Taking V_{dc} as the base for per unit calculations, the following vectors can be written:

$$v_x = v_4 = (1 + j0)\,\text{p.u.}, \qquad v_y = v_6 = \left(\frac{1}{2} + j\frac{\sqrt{3}}{2}\right)\,\text{p.u.},$$

$$V_{\max} = \frac{\sqrt{3}}{2}\,\text{p.u.} \tag{4}$$

Substituting the above vectors in Eq. (3) gives:

$$\frac{\sqrt{3}}{2} M\cos(\alpha) = d_x + \frac{1}{2}d_y, \qquad \frac{\sqrt{3}}{2} M\sin(\alpha) = \frac{\sqrt{3}}{2} d_y \tag{5}$$

Solving for the duty ratios from the above equations yield:

$$d_x = M\sin(60^\circ - \alpha) \quad \text{and} \quad d_y = M\cos(\alpha) \tag{6}$$

Also, the duration of the zero vector from Eq. (2) is given by

$$d_z = 1 - d_x - d_y \tag{7}$$

The simple algebric formulas Eqs. (6) and (7), allow real-time computation of the duty ratios of the consecutive logic states of the inverter.

These same equations apply to any sector, since the d–q reference frame can be aligned with any base vector.

2.1. Realization of the PWM switching pattern

After calculating the required PWM duty ratios d_x, d_y and d_z for a particular reference voltage V^*, the appropriate compare

values for the compare registers need to be calculated. A set of three new compare values (T_a, T_b and T_c) needs to be calculated every PWM period (50 μS) to generate the switching pattern. The compare values T_a, T_b and T_c can be written as

$$T_a = \frac{T - d_x - d_y}{2} \tag{8}$$

$$T_b = d_x + T_a \tag{9}$$

$$T_c = T - T_a \tag{10}$$

The calculated compare values are loaded into PWM compare registers and the DSP controller updates the duty ratio at the beginning of the next PWM cycle.

3. The proposed modified SVPWM

The assumption in the SVPWM method described above is the stiffness of the inverter dc bus voltage. As discussed in the introduction, a constant and ripple free dc voltage is not ensured at the output of alternate energy sources. In view of this a modified SVPWM method is presented here that will counter the dc-bus ripple effect in order to maintain the quality of the inverter output voltage. The actual dc bus voltage, V_{ripple} can be written as

$$V_{dc} = K_{ripple}\, V_{ripple} \tag{11}$$

where V_{dc} is the desired or reference dc bus voltage and K_{ripple} is the ripple factor that varies with dc-bus voltage ripple. The ripple factor (K_{ripple}) is utilized to modify the duty ratio of the different inverter states. Let us denote the duty ratios required for dc ripple compensation as d_{x_new} and d_{y_new}. Eq. (5) can be rewritten as

$$\frac{\sqrt{3}}{2} M K_{ripple} \cos(\alpha) = d_{x\_new} + \frac{1}{2} d_{y\_new} \tag{12}$$

$$\frac{\sqrt{3}}{2} M K_{ripple} \sin(\alpha) = \frac{\sqrt{3}}{2} d_{y\_new} \tag{13}$$

Solving for the modified duty ratios:

$$d_{x\_new} = M K_{ripple} \sin(60^\circ - \alpha) \tag{14}$$

$$d_{y\_new} = M K_{ripple} \sin(\alpha) \tag{15}$$

It is clear from the Eqs. (14) and (15) that the new duty ratios are modified by the extent of dc ripple present in the dc-bus voltage. These duty ratios will be continuously updated to minimize the effect of dc-bus voltage ripple.

The block diagram of the DSP based interface is shown in Fig. 3. A three-phase pulse width modulated (PWM) inverter acts as the interface between the alternate energy system (which produces or stores electric energy in dc form) and the ac power system. The dc bus voltage information is fed into the DSP controller that generates the PWM control signals for the inverter switches and maintains the stiffness of the ac voltages regardless of variation in the input dc bus voltage.

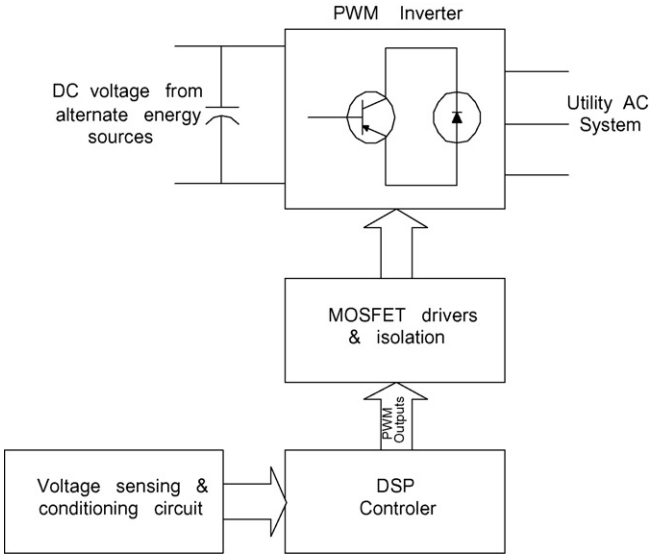


Fig. 3. Block diagram of the proposed DSP based interface.

4. Experimental setup and results

Fig. 4 shows the laboratory setup used to verify the proposed control algorithm. ac input from a variac is fed into an uncontrolled rectifier. The output of the rectifier is connected as an input to the inverter through a dc-link capacitor. Texas Instruments DSP TMS320F243 was used as the controller, to generate the PWM signals for the inverter. Three phase balanced lamp loads were connected at the inverter output. In order to model the unregulated dc voltage, a dc-link 47 μF capacitor is used. This introduces a ripple in the dc bus voltage, which is applied as an input to the inverter. Fig. 5 shows the dc voltage and its frequency spectrum with a 47 μF dc link capacitor. It can be observed that the dc voltage is not constant but is varying with time. It can also be seen from the time domain signal in Fig. 5 that the dc bus voltage varies between 25 and 34 V and the presence of the second harmonic (120 Hz) ripple component is evident from the corresponding frequency spectrum.

The ripple introduced in the dc input voltage gets reflected at the inverter output causing the fundamental component in the inverter output voltage to vary with time. The experimental observation of the variation can be illustrated with the help of Fig. 6. Fig. 6(a) is taken at the time when the fundamental component is at its minimum value (11.25 V) and Fig. 6(b) is taken when the fundamental component is at its maximum value (13 V). The dc bus voltage is sensed and the conditioned digital version is fed into the DSP controller by an on chip A/D converter. The DSP program implements the proposed modified SVPWM algorithm as described in section III and generates

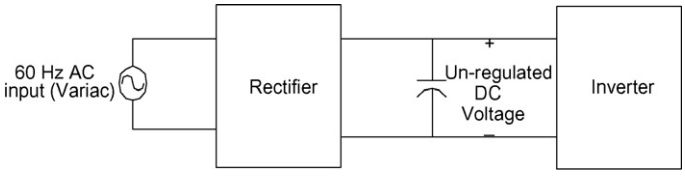


Fig. 4. Block diagram of the proof of concept laboratory setup.

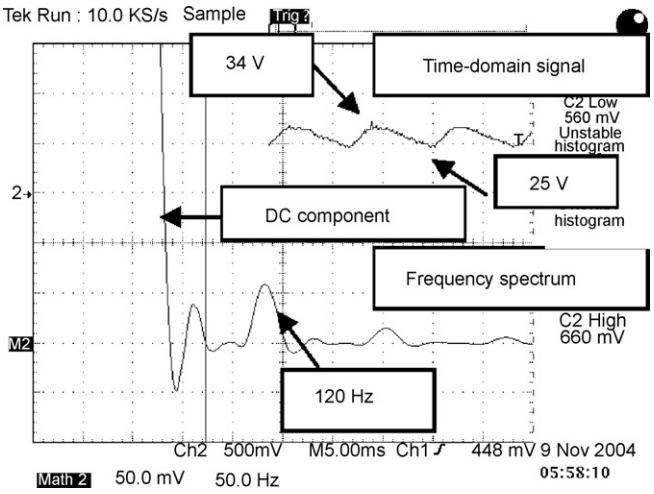
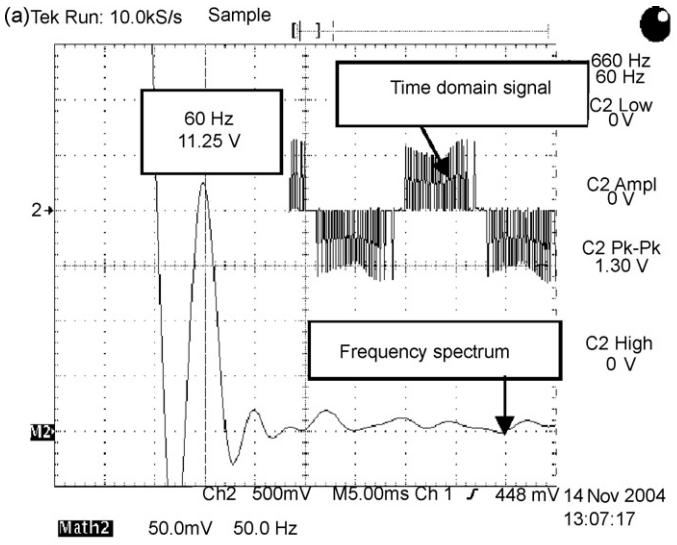


Fig. 5. dc-Bus voltage and its frequency spectrum with a 47 μF dc link capacitor.



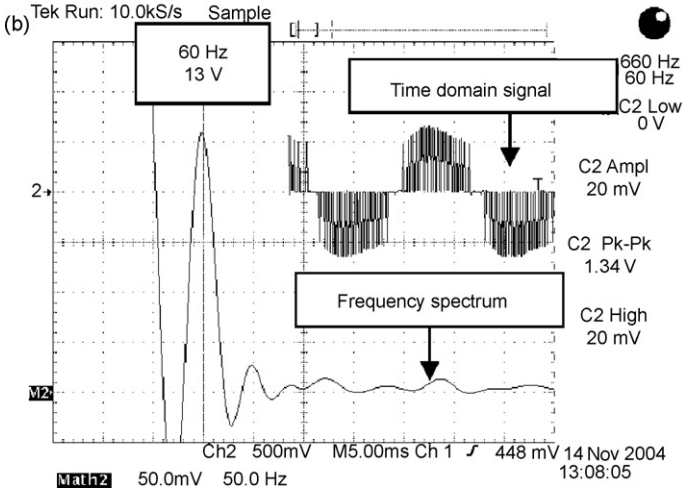
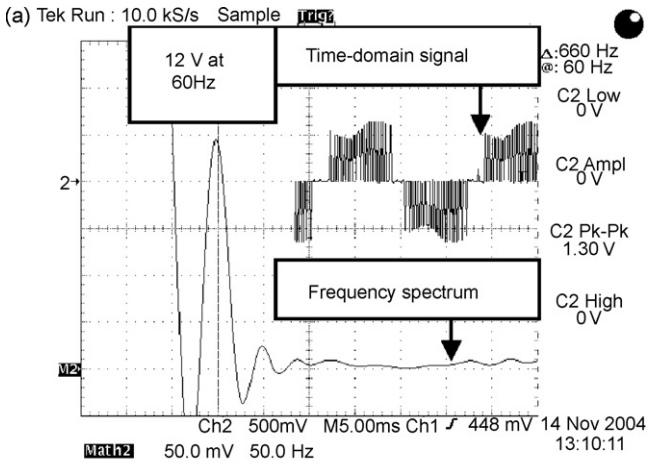


Fig. 6. Inverter line to line output voltage and its frequency spectrum at two instants of time.



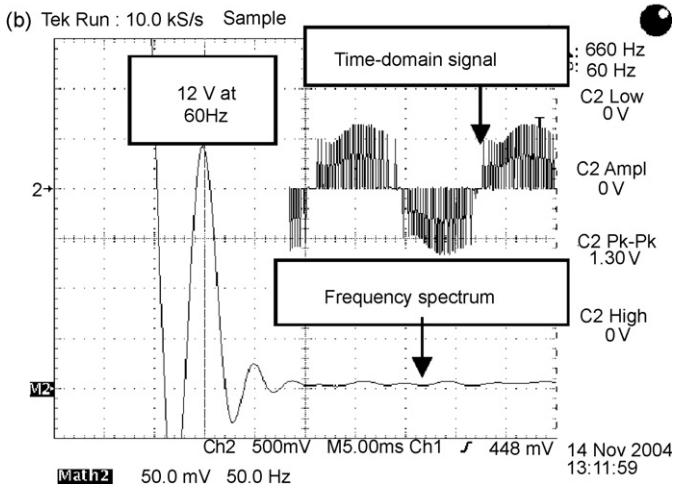


Fig. 7. Inverter line to line output voltage and its frequency spectrum with the modified SVPWM control.

the PWM control signals for the inverter switches. Fig. 7 shows experimental observations of the inverter line to line output voltage taken at two instants of time when the dc bus voltage is well below its average value (Fig. 7(a)) and when the dc bus voltage is well above its average value (Fig. 7(b)). It can be seen that unlike Fig. 6, the output voltage magnitude (fundamental component) is maintained at 12 V regardless of the variation in the input dc bus voltage.

Fig. 8 shows a plot of the recorded experimental data of the inverter output voltage magnitude with the dc bus voltage varying in the range of 25–34 V (when the dc-link capacitor is 47 μF), both with and without the proposed correction algorithm in effect. It can be seen that without correction the output voltage increases as the dc bus voltage is increased but with the modified SVPWM correction in place the output voltage magnitude is maintained constant (at 12 V) regardless of the dc bus voltage.

Fig. 9 shows a plot of the recorded experimental data when the dc bus voltage is manually varied over a wider range (55–110 V). This was done by using the input variac in the laboratory setup. It can be seen from the plot in Fig. 9 that with modified SVPWM control in effect, the output voltage magnitude is

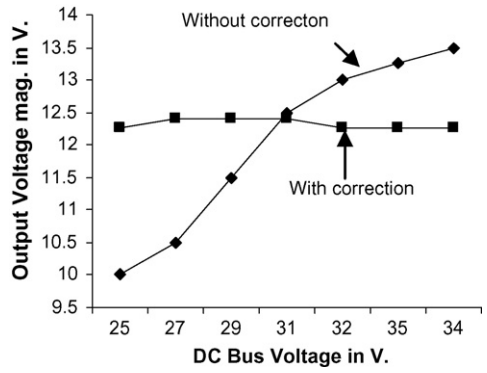


Fig. 8. Inverter output voltage magnitude when the dc bus voltage varies in the range of 25–34 V (with 47 μF dc-link capacitor).

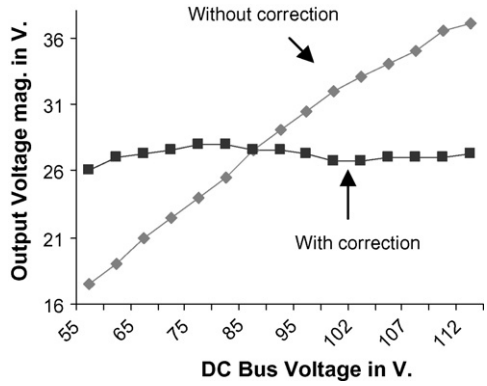


Fig. 9. Inverter output voltage magnitude when the dc bus voltage is varied in the range of 55–110 V.

maintained constant (at 26 V) even when the input dc voltage is varied over a wide range.

5. Conclusions

A modified space vector pulse width modulation (SVPWM) technique is presented that will make the output of utility interactive inverters immune to the variations in the dc input voltage obtained from alternate sources of energy. With the proposed SVPWM strategy incorporated in the DSP controller, high quality output voltages can be maintained at the point of common coupling. Results from an experimental setup are presented to identify the problem and demonstrate the proposed scheme and its use.

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